CLAIMS

The invention claimed is:

1. A method of forming a semiconductor structure, comprising:

providing a semiconductor substrate having a first doped semiconductor region and a second doped semiconductor region over the first doped semiconductor region, one of the first and second doped semiconductor regions being a p-type region and the other being an n-type region;

forming a trench extending through the second doped semiconductor region and into the first doped semiconductor region, the trench having a sidewall comprising the first and second doped semiconductor regions;

forming a silicide from the trench sidewall, the silicide being within the second doped semiconductor region and not within the first doped semiconductor region; and

forming electrically insulative material within the trench to cover the silicide.

2. The method of claim 1 wherein the electrically insulative material is a second electrically insulative material, the method further comprising:

forming a first electrically insulative material within the trench to partially fill the trench, the partially-filled trench being filled to above an elevational level of an uppermost portion of the first doped semiconductor region along the sidewall;

forming a metal-containing layer within the partially-filled trench and along the second doped semiconductor region of the sidewall; and

reacting at least some of the metal from the metal-containing layer with the second doped semiconductor region of the sidewall to form the silicide.

3. The method of claim 2 wherein the metal-containing layer comprises one or more of Co, Ni, Ta, W and Ti.

4. The method of claim 2 wherein the first and second electrically insulative materials are the same as one another in chemical composition.

5. The method of claim 4 wherein the first and second electrically insulative materials both comprise silicon dioxide.

6. The method of claim 4 wherein the first and second electrically insulative materials both consist of silicon dioxide.

7. The method of claim 1 wherein the first doped semiconductor region is the p-type region.

8. The method of claim 1 wherein the first doped semiconductor region is the n-type region.

9. The method of claim 1 wherein the first and second doped semiconductor regions comprise conductively-doped silicon.

10. The method of claim 1 wherein the first and second doped semiconductor regions comprise conductively-doped monocrystalline silicon.

11. The method of claim 1 wherein the first and second doped semiconductor regions consist essentially of conductively-doped monocrystalline silicon.

12. The method of claim 1 wherein the first and second doped semiconductor regions consist of conductively-doped monocrystalline silicon.

13. The method of claim 1 further comprising incorporating the silicide into a bitline.

14. A method of forming a semiconductor structure, comprising:

providing a semiconductor material having a trench extending therein;

forming a first electrically insulative material within a bottom portion of the trench to partially fill the trench, the partially-filled trench having a sidewall comprising the semiconductor material;

incorporating the semiconductor material of the sidewall into a silicide, the silicide being a line extending along the trench; and

filling the trench with a second electrically insulative material to cover the silicide.

15. The method of claim 14 further comprising incorporating the silicide line into a bitline.

16. The method of claim 14 further comprising:

forming a metal-containing layer over the substrate, within the partially-filled trench and along the sidewall; and

forming the silicide from metal of the metal-containing layer by reacting metal from the metal-containing layer with the semiconductor material of the sidewall.

17. The method of claim 14 further comprising:

forming a metal-containing layer over the substrate, within the partially-filled trench and along the sidewall;

forming the silicide from metal of the metal-containing layer by reacting some of the metal from the metal-containing layer with the semiconductor material of the sidewall, some of the metal of the metal-containing layer not reacting to form the silicide; and

removing the unreacted metal of the metal-containing layer.

18. The method of claim 14 wherein:

the semiconductor material comprises a first doped region and a second doped region over the first doped region;

one of the first and second doped regions is a p-type region and the other is an n-type region;

the trench extends entirely through the second doped region and has a portion extending within the first doped region; and

the first electrically insulative material entirely fills the portion of the trench that is within the first doped region.

19. The method of claim 18 wherein the first doped region is the n-type region.

20. The method of claim 18 wherein the first doped region is the p-type region.

21. The method of claim 14 wherein the first and second electrically insulative materials are the same as one another in chemical composition.

22. The method of claim 14 wherein:

said sidewall is one of a pair of opposing sidewalls within the partially-filled trench;

the silicide line is a first silicide line;

semiconductor material of the other of said pair of opposing sidewalls is incorporated into a silicide to form a second silicide line extending along the trench; and

the second silicide line is spaced from the first silicide line.

23. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate, the semiconductor substrate having a semiconductive material surface;

forming a trench extending into the substrate;

forming a silicide line along a sidewall of the trench;

depositing a first electrically insulative material within the trench to cover the silicide line;

forming a patterned second electrically insulative material over the silicide line and the first electrically insulative material; the patterned second electrically insulative material having an opening extending therethrough to expose a portion of the semiconductive material surface of the semiconductor substrate;

forming a pillar of conductively-doped semiconductor material within the opening; and

replacing at least some of the second electrically insulative material with a conductive material.

24. The method of claim 23 wherein the semiconductor substrate comprises a monocrystalline semiconductor material along said surface, and wherein the pillar of conductively-doped semiconductor material is epitaxially grown from the monocrystalline semiconductor material of the substrate.

25. The method of claim 24 wherein the monocrystalline semiconductor material of the substrate comprises silicon.

26. The method of claim 24 wherein the monocrystalline semiconductor material of the substrate consists of silicon.

27. The method of claim 24 wherein the pillar of conductively-doped semiconductor material is doped to comprise a first type region between a pair of second type regions, with one of the first and second types being n-type and the other being p-type.

28. The method of claim 27 wherein the first type region is the n-type region.

29. The method of claim 27 wherein the first type region is the p-type region.

30. The method of claim 23 wherein:

the substrate comprises a first doped region and a second doped region over the first doped region, one of the first and second doped regions being p-type and the other being n-type;

the trench extends through the second doped region and into the first doped region; and

the silicide is within the second doped region and not within the first doped region of the substrate.

31. The method of claim 30 wherein the first doped region is the p-type region.

32. The method of claim 30 wherein the first doped region is the n-type region.

33. The method of claim 23 wherein:

the substrate comprises a first doped region and a second doped region over the first doped region, one of the first and second doped regions being p-type and the other being n-type;

the trench extends through the second doped region and into the first doped region;

a filler material is formed within the bottom of the trench prior to forming the silicide;

the filler material completely fills a portion of the trench which extends into the second doped region;

a metal-containing layer is formed within the trench and over the filler material; and

metal from the metal-containing layer is reacted with substrate of the second doped region to form the silicide.

34. The method of claim 23 wherein:

the pillar of conductively-doped semiconductor material comprises a channel region between a pair of source/drain regions;

the conductive material which replaces at least some of the second electrically insulative material comprises a transistor gate which gatedly connects the source/drain regions to one another through the channel region and is incorporated into a wordline; and

the silicide is electrically connected with one of the source/drain regions and is incorporated into a bitline.

35. The method of claim 34 wherein said one of the source/drain regions which is electrically connected with the silicide is a first source/drain region, wherein the other of the source/drain regions of the pair of source/drain regions is a second source/drain region and is electrically connected with a capacitor, and wherein the combination of the transistor gate, capacitor, source/drain regions and channel regions forms a DRAM unit cell.

36. The method of claim 35 wherein the DRAM unit cell is formed simultaneously with a plurality of other DRAM unit cells and incorporated with said other DRAM unit cells in a DRAM array.

37. The method of claim 36 further comprising incorporating the DRAM array within an electronic device.

38. A method of forming a semiconductor memory device, comprising:

providing a semiconductor substrate, the semiconductor substrate having a semiconductive material upper surface;

forming a trench extending through the upper surface and into the substrate;

forming a silicide bitline along a sidewall of the trench;

depositing a first electrically insulative material within the trench to cover the bitline;

forming a patterned second electrically insulative material over the bitline and first electrically insulative material; the patterned second electrically insulative material having an opening extending therethrough to expose a portion of the semiconductive material upper surface;

forming a vertically-extending pillar of conductively-doped semiconductor material within the opening, the pillar being doped to comprise a pair of first type source/drain regions on vertically opposed sides of a second type channel region, one of the first and second types being p-type and the other being n-type, the pair of source/drain regions being a first source/drain region and a second source/drain region, the first source/drain region being in electrical connection with the bitline;

forming a gate dielectric around the pillar;

replacing at least some of the second electrically insulative material

with a conductive wordline material, the conductive wordline material laterally surrounding the pillar and being separated from the pillar by the gate dielectric; and

forming a charge storage device in electrical connection with the second source/drain region.

39. The method of claim 38 wherein the charge storage device is a capacitor.

40. The method of claim 39 wherein the capacitor, source/drain regions and channel region are together incorporated within a DRAM unit cell.

41. The method of claim 40 wherein the DRAM unit cell is one of a plurality of DRAM unit cells which are formed utilizing the same processing as one another.

42. The method of claim 41 wherein the DRAM unit cell is one of a plurality of DRAM unit cells which are formed utilizing the same processing as one another.

43. The method of claim 42 further comprising incorporating the plurality of DRAM unit cells into an electronic system.

44. The method of claim 38 wherein the opening extending through the second electrically insulative material to the exposed portion of the semiconductive material surface is a second opening, the method further comprising:

forming an etch stop material over the substrate;

forming the second electrically insulative material over the etch stop material and patterning the second electrically insulative material to form the patterned second electrically insulative material having a first opening extending therethrough to the etch stop, the second electrically insulative material forming a periphery of the opening;

forming an anistropically etched spacer along the periphery to narrow the first opening; and

extending the narrowed first opening to the semiconductive material upper surface to form the second opening.

45. The method of claim 44 wherein the second electrically insulative material is formed directly against the etch stop.

46. The method of claim 44 further comprising forming a low-k dielectric material over the substrate and forming the etch stop over and directly against the low k dielectric material.

47. The method of claim 46 wherein the low-k dielectric material comprises silicon dioxide and wherein the etch stop comprises one or both of aluminum oxide and hafnium oxide.

48. The method of claim 44 further comprising, after forming the vertically-extending pillar:

selectively removing the anistropically-etched spacer relative to the second electrically insulative material to form a space between the second electrically insulative material and the vertically-extending pillar; and

forming the gate dielectric within the space.

49. The method of claim 48 the gate dielectric comprises silicon dioxide, wherein the vertically-extending pillar comprises silicon, and wherein the gate dielectric is formed by exposing a surface of the vertically-extending pillar to oxidizing conditions.

50. The method of claim 48 the gate dielectric consists of silicon dioxide and is formed by depositing silicon dioxide along a surface of the vertically-extending pillar.

51. The method of claim 48 the patterned second electrically insulative material comprises silicon dioxide and wherein the anisotropically-etched spacer comprises silicon nitride.

52. A semiconductor construction, comprising:

a first doped semiconductor region;

a second doped semiconductor region over the first doped semiconductor region, one of the first and second doped semiconductor regions being a p-type region and the other being an n-type region;

an isolation region extending entirely through the second doped semiconductor region and partially into the first semiconductor region; and

a silicide line extending along and directly against the isolation region, the silicide line being entirely contained between the isolation region and the second doped semiconductor region.

53. The construction of claim 52 wherein the first and second doped semiconductor regions are the n-type and p-type regions, respectively.

54. The construction of claim 52 wherein the first and second doped semiconductor regions are the p-type and n-type regions, respectively.

55. The construction of claim 52 wherein the first and second doped semiconductor regions both consist of doped silicon.

56. The construction of claim 52 wherein the first and second doped semiconductor regions both consist of doped monocrystalline silicon.

57. The construction of claim 52 wherein the isolation region comprises silicon dioxide.

58. The construction of claim 52 wherein the silicide is selected from the group consisting of cobalt silicide, nickel silicide, titanium silicide, tungsten silicide, tantalum silicide, and mixtures thereof.

59. A semiconductor construction, comprising:

a first doped semiconductor region;

a second doped semiconductor region over the first doped semiconductor region, one of the first and second doped semiconductor regions being a p-type region and the other being an n-type region;

an isolation region extending entirely through the second doped semiconductor region and partially into the first doped semiconductor region, the isolation region being a line having a pair of opposing sidewalls, one of the sidewalls being a first sidewall and the other being a second sidewall;

a first silicide line extending along and directly against the first sidewall, the first silicide line being in direct physical contact with the second doped semiconductor region but not in direct physical contact with the first doped semiconductor region; and

a second silicide line extending along and directly against the second sidewall, the second silicide line being in direct physical contact with the second doped semiconductor region but not in direct physical contact with the first doped semiconductor region.

60. The construction of claim 59 wherein the first and second silicide lines are entirely contained between the isolation region and the second doped semiconductor region.

61. The construction of claim 59 wherein the first and second doped semiconductor regions are n-type and p-type, respectively.

62. The construction of claim 59 wherein the first and second doped semiconductor regions are p-type and n-type, respectively.

63. The construction of claim 59 wherein the isolation region comprises silicon dioxide.

64. The construction of claim 59 wherein the isolation region is a single homogenous composition.

65. The construction of claim 59 wherein the isolation region has a lower portion and an upper portion which differ in chemical composition relative to one another.

66. The construction of claim 65 wherein the lower portion comprises an entirety of the isolation region within the first doped semiconductor region and part of the isolation region within the second doped semiconductor region.

67. A semiconductor construction, comprising:

a semiconductor substrate comprising a conductively-doped semiconductive material;

a trenched isolation region within the conductively-doped semiconductive material, the trenched isolation region having a sidewall;

a silicide-containing bitline between the sidewall of the trenched isolation region and the conductively-doped semiconductive material;

a dielectric material over the silicide-containing bitline and trenched isolation region;

a wordline over the dielectric material; and

a vertically-extending pillar proximate the wordline and comprising a channel region vertically between a pair of source/drain regions, the wordline comprising a transistor gate which gatedly connects the source/drain regions to one another through the channel region, one of the pair of source/drain regions being electrically connected to the bitline.

68. The construction of claim 67 wherein the conductively-doped semiconductive material of the substrate comprises silicon.

69. The construction of claim 67 wherein the vertically-extending pillar is not directly over the bitline.

70. The construction of claim 67 wherein the conductively-doped semiconductive material comprises monocrystalline semiconductive material, and wherein the vertically-extending pillar comprises a monocrystalline extension of said monocrystalline semiconductive material.

71. The construction of claim 67 wherein the source/drain regions of the vertically-extending pillar are n-type regions and the channel region of the vertically-extending pillar is a p-type region.

72. The construction of claim 67 wherein the source/drain regions of the vertically-extending pillar are p-type regions and the channel region of the vertically-extending pillar is an n-type region.

73. The construction of claim 67 wherein the dielectric material consists of silicon dioxide.

74. The construction of claim 67 wherein:

the substrate comprises a first doped region and a second doped region over the first doped region, one of the first and second doped regions being p-type and the other being n-type, the conductively-doped semiconductive material being the second doped region;

the trenched isolation region extends through the second doped region and into the first doped region; and

the silicide-containing bitline is within the second doped region and not within the first doped region of the substrate.

75. The construction of claim 74 wherein the first doped region is the p-type region.

76. The construction of claim 74 wherein the first doped region is the n-type region.

77. The construction of claim 67 wherein said one of the source/drain regions which is electrically connected with the silicide-containing bitline is a first source/drain region, wherein the other of the source/drain regions of the pair of source/drain regions is a second source/drain region and is electrically connected with a capacitor, and wherein the combination of the transistor gate, capacitor, source/drain regions and channel regions forms a DRAM unit cell.

78. A DRAM array comprising the DRAM unit cell of claim 77 together with a plurality of other DRAM unit cells substantially identical to the DRAM unit cell of claim 76.

79. An electronic device comprising the DRAM array of claim 78.

80. A semiconductor construction, comprising:

a semiconductor substrate, the semiconductor substrate having a semiconductive material upper surface;

an isolation region extending into the substrate;

a silicide-containing bitline between the isolation region and the substrate;

a spaced pair of wordlines over the bitline and isolation region, one of the pair of wordlines being a first wordline and the other being a second wordline;

an electrically insulative line between the spaced wordlines;

a first vertically-extending pillar of conductively-doped semiconductor material extending upwardly from the semiconductive material upper surface, the first vertically-extending pillar extending upwardly through the first wordline, the first vertically-extending pillar comprising a pair of first type source/drain regions on vertically opposed sides of a second type channel region, one of the first and second types being p-type and the other being n-type, the pair of source/drain regions being a first source/drain region and a second source/drain region, the first source/drain region being in electrical connection with the bitline;

a second vertically-extending pillar of conductively-doped semiconductor material extending upwardly from the semiconductive material upper surface, the second vertically-extending pillar extending upwardly through the second wordline, the second vertically-extending pillar comprising a pair of first type

source/drain regions on vertically opposed sides of a second type channel region, the pair of source/drain regions of the second vertically-extending pillar being a third source/drain region and a fourth source/drain region, the third source/drain region being in electrical connection with the bitline;

a first gate dielectric around the first vertically-extending pillar and separating the first vertically-extending pillar from the first wordline;

a second gate dielectric around the second vertically-extending pillar and separating the second vertically-extending pillar from the second wordline;

a first charge storage device in electrical connection with the second source/drain region; and

a second charge storage device in electrical connection with the fourth source/drain region.

81. The construction of claim 80 wherein the first and second charge storage devices are capacitors.

82. The construction of claim 81 wherein the capacitors, source/drain regions and channel regions are incorporated within a pair of DRAM unit cells.

83. The DRAM unit cells of claim 82 wherein each of the unit cells, excluding the capacitors, is a $4F^2$ device.

84. A DRAM array comprising the DRAM unit cells of claim 82.

85. An electronic system comprising the DRAM array of claim 84.

86. The construction of claim 81 wherein the electrically insulative line comprises silicon dioxide.

87. The construction of claim 81 wherein the electrically insulative line comprises silicon dioxide over a high-k dielectric material.

88. The construction of claim 81 wherein the electrically insulative line consists of silicon dioxide over a high-k dielectric material.

89. The construction of claim 88 wherein the high-k dielectric material consists of one or both of aluminum oxide and hafnium oxide.

90. The construction of claim 81 further comprising a high-k dielectric material between the isolation region and the electrically insulative line.

91. The construction of claim 90 wherein the high-k dielectric material consists of one or both of aluminum oxide and hafnium oxide.

92. The construction of claim 90 further comprising a low-k dielectric material between the isolation region and the high-k dielectric material.

93. The construction of claim 92 wherein the low-k dielectric material is between the first and second wordlines and the semiconductive material upper surface of the substrate.

94. The construction of claim 93 wherein the high-k dielectric material is not between the first and second wordlines and the semiconductive material upper surface of the substrate.

95. The construction of claim 92 wherein the low-k dielectric material comprises silicon dioxide and wherein the high-k dielectric material comprises one or both of aluminum oxide and hafnium oxide.

96. The construction of claim 92 wherein the low-k dielectric material consists of silicon dioxide.

97. The construction of claim 81 wherein the first and second gate dielectrics comprise silicon dioxide.

98. The construction of claim 81 wherein the first and second gate dielectrics consist of silicon dioxide.

99. The construction of claim 81 wherein the first and second wordlines comprise conductively-doped silicon.

100. The construction of claim 81 wherein the first and second wordlines consist of conductively-doped silicon.

101. The construction of claim 81 wherein the silicide-containing bitline consists of the silicide.